REMARKS

Applicants appreciate the thorough examination of the present application that is reflected in the Official Action of June 10, 2004. Applicants also appreciate the Examiner's indication that Claims 10-18, 20, 27, 38 and 39 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. However, these claims have not been rewritten in independent form, because Applicants respectfully submit that all of the pending claims as filed are allowable over the cited reference, U.S. Patent 6,122,274 to Kumar. The reasons for allowability of all the pending claims will now be described.

Claims 1-20 Are Patentable Over Kumar

Independent Claim 1 recites:

> 1. An integrated circuit First-In-First-Out (FIFO) memory device comprising:
> a FIFO memory that is divisible into up to a predetermined number of independent FIFO queues;
> a register file including the predetermined number of words, a respective word of which is configured to store one or more parameters for a respective one of the FIFO queues;
> an indexer that is configured to index into the register file to access a respective word that corresponds to a respective FIFO queue that is accessed; and
> a controller that is responsive to the respective word that is accessed and that is configured to control access to the respective FIFO queue based upon at least one of the one or more parameters that is stored in the respective word.

As will be described below, the elements of Claim 1 are not described or suggested by Kumar.

In particular, Claim 1 recites "a FIFO memory that is divisible into up to a predetermined number of independent FIFO queues". For example, as noted in the present application at Page 2, lines 19-21:

> Accordingly, in a single integrated circuit chip, anywhere between one and the predetermined number, such as up to 32 or more, of discrete FIFO queues can be set up.

In sharp contrast, Figure 2 of Kumar and the accompanying description describes an ATM switch with decentralized pipeline control having a fixed number **m** of memory modules **40$_1$**-

40$_m$. Accordingly, the above-quoted recitation of Claim 1 is simply not described or suggested in Kumar.

Moreover, the Official Action states that the claimed register file corresponds to Kumar's elements **10** and **30**. As recited in Claim 1, the register file includes "the predetermined number of words", so that, for example, if the FIFO memory is divisible into up to 32 queues, then 32 words are present in the register file. Moreover, Claim 1 recites that a respective word of the register file is configured to store "one or more parameters for a respective one of the FIFO queues".

In sharp contrast, element **10** of Kumar is a "header processing circuit", which is used for "extraction of the output line destination address denoted by d", as noted in Kumar Column 6, lines 60-61. As also noted in Kumar Column 7, lines 1-3, the header processing circuits **10** attach a self-routing tag to the incoming ATM cells. Moreover, element **30** of Kumar corresponds to input modules. As noted by Kumar, Column 7, lines 22-29:

> The input modules **30$_1$**, **30$_2$**, . . . **30$_m$** can be used for multiple purposes however, the primary purpose of the input modules **30$_1$**, **30$_2$**, . . . **30$_m$** is to hold a received cell for a predetermined time period before being stored in the respective memory modules. Another function of modules **30$_1$**, **30$_2$**, . . . **30$_m$** is to hold a received ATM cell and provide the parameters j and k information from the cell's self-routing tag to memory controllers **50$_1$**, **50$_2$**, . . . **50$_m$**. (Emphasis added.)

Accordingly, neither Kumar's header processing circuits **10**, nor Kumar's input modules **30**, include "the predetermined number of words" as recited in Claim 1, and a respective word does not store "one or more parameters for a respective one of the FIFO queues" as recited in Claim 1. Thus, the claimed register file is not described or suggested by Kumar's header circuits **10** and/or input modules **30**.

Claim 1 also recites an indexer. The Official Action states that the input modules **30** correspond to the indexer. However, as was already described by the above-quoted portion of Kumar, the input modules **30** hold a received cell for a predetermined time period and provide the parameters j and k for the cell's self-routing tag. An indexer "that is configured to index into the register file to access a respective word that corresponds to a respective FIFO queue that is accessed", as recited in Claim 1, is simply not described or suggested.

Finally, Claim 1 recites a controller. The Official Action states that memory controllers **50** of Kumar correspond to the controller that is recited in Claim 1. However, as noted in Kumar Column 7, lines 29-32:

> The memory controllers use the parameter j to write the received ATM cell in the j^{th} memory-location of the corresponding memory modules 40_1, 40_2, . . . 40_m.

Accordingly, the memory controllers are not "configured to control access to the respective FIFO queue based upon at least one of the one or more parameters that is stored in the respective word". For at least the reasons described above, the recitations of the FIFO memory, register file, indexer and controller of Claim 1 are not described or suggested by Kumar.

At Page 3 of the Official Action, the Official Action appears to concede that "Kumar does not expressly teach a register file and indexer". Notwithstanding this assertion, the Official Action states at Page 3:

> However, it would have been obvious to one of ordinary skill that *Kumar* teaches a method of a register file and indexer with the header processing circuit (10) and the input module (30). Specifically, both are configured to store one or more parameters...associated with the incoming packets. Each independent memory modules each have a corresponding controller that is configured to control access to the respective memory modules. Further, it would have been obvious to one of ordinary skill that the parameter word tags i, k, j are used by each of the controller(s) for determining where to output the stored packets via the memory module(s).

In response, Applicants respectfully submit that the claimed register file is "configured to store one or more parameters for a respective one of the FIFO queues" rather than "one or more parameters...associated with the incoming packets", as stated in the above-quoted portion of the Official Action. Moreover, the parameter word tags i, j and k of Kumar "provide a set of self-routing parameters", as noted in Kumar Column 6, lines 65-67, that are attached as a self-routing tag to the incoming ATM cells, as noted in Kumar Column 7, lines 1-3. These parameters i, j and k do not relate to "parameters for a respective one of the FIFO queues", as recited in Claim 1, but are, rather, parameters as to routing of the data itself. Accordingly, even if it would have been obvious to one of ordinary skill in the art that "the parameter word tags i, j, k are used by each of the controller(s) for determining where to output the stored packets via the memory module(s)", as stated by the Official Action, this would not suggest the recitations of Claim 1.

In conclusion, since Kumar describes an ATM switch, Kumar describes memory modules, memory controllers and the like. However, Applicants have now shown that none of the four elements of Claim 1 are described or suggested by Kumar. Accordingly, Claim 1, and Claims 2-20 that depend therefrom, are patentable over Kumar.

Many of the dependent claims also are separately patentable. In particular, the Official Action has acknowledged that Claims 10-18 and 20 are independently patentable. Moreover, many of the other dependent claims are separately patentable. For example, Claim 3 recites:

> 3. An integrated circuit FIFO memory device according to Claim 1 wherein the one or more parameters comprise a number of words read, a number of words written, a number of packets read, a number of packets written, a location of a next word to be read, a location of a next word to be written, a start address and/or an end address for the respective queue.

As already was described above, the parameters i, j and k of Kumar are routing parameters for an incoming ATM packet, and do not describe or suggest any of the FIFO queue packets that are recited in Claim 3. Accordingly, Claim 3 is separately patentable.

Moreover, Claim 4 recites:

> 4. An integrated circuit FIFO memory device according to Claim 1 wherein the one or more parameters comprise mask values that are used to generate a full, almost full and/or almost empty flag for the respective queue.

The Official Action states that Figure 8 of Kumar describes the "one or more parameters comprise a mask value that generates a[n] empty or full signal". However, as noted in Kumar Column 14, lines 23-27:

> The ATM cell read operation performed by the memory controllers **50_1**, **50_2**, . . . **50_m** is shown by a flow chart steps **800-806** in FIG. 8. The memory controllers **50_1**, **50_2**, . . . **50_m** also use a sliding-window counter in the read processor **56_1**, **56_2**, . . . **56_m**.

Accordingly, Kumar Figure 8 does not describe or suggest storing in a register file, parameters that comprise mask values that are used to generate an almost full and/or almost empty flag for the respective queue. Claim 4 is, therefore, independently patentable.

Finally, as to Claims 6-9, the Official Action states at the top of Page 4:

> As per claims 6-9 *Kumar* obviously teaches that based on the parameters the controller is configured to control the reading and/or writing from the respective FIFO queue based on the given parameters.

Applicants wish to reiterate that Kumar's parameters i, j and k are routing parameters related to an incoming cell, rather than internal parameters that govern reading and/or writing of a FIFO queue. Accordingly, Claims 6-9 are independently patentable.

Claims 21-27 Are Patentable Over Kumar

Claim 21 recites:

> 21. An integrated circuit First-In-First-Out (FIFO) memory device comprising:
> a FIFO memory;
> a data input port;
> a data output port;
> a FIFO controller that is configured to operate the FIFO memory as from one up to a predetermined number greater than one of independent FIFO queues;
> a data input system that is configured to write input data from the input port into a first selected one of the independent FIFO queues; and
> a data output system that is configured to read data from a second selected one of the independent FIFO queues.

As was already described in connection with the rejection of Claim 1, Kumar does not describe a FIFO memory that is configurable to operate as from one up to a predetermined number greater than one of independent FIFO queues. Rather, Kumar describes a FIFO memory that is fixedly configured to operate with **m** FIFO queues. Accordingly, Kumar does not describe or suggest "a FIFO controller that is configured to operate the FIFO memory as from one up to a predetermined number greater than one of independent FIFO queues", as recited in Claim 21. Nor would it be obvious to provide a reconfigurable FIFO memory based on the fixed FIFO memory of Kumar. Accordingly, Claim 21 and dependent Claims 22-27 that depend therefrom, are patentable over Kumar. Moreover, the Official Action has also acknowledged that Claim 27 is independently patentable.

Moreover, many of the other dependent claims are separately patentable. In particular, Claim 22 is independently patentable for at least the reasons that were described above in connection with the register file of Claim 1. This analysis will not be repeated again for the sake of brevity. Claims 23 and 24 are patentable at least for the same reasons that were described above in connection with Claims 3 and 4. This analysis also will not be repeated for the sake of brevity. Claim 26 is independently patentable for at least the reasons that were described in connection with the register file and the indexer of Claim 1. This analysis also will not be repeated for the sake of brevity. For at least these reasons, Claims 22-24 and 26 are independently patentable.

Claims 28-32 Are Patentable

Claim 28 includes the same recitations of "a register file", "an indexer" and "a controller" as Claim 1. Accordingly, Claim 28 is patentable for the same reasons that were described above in connection with these elements of Claim 1. This analysis will not be repeated for the sake of brevity. Claims 29-32 are patentable at least per the patentability of Claim 28 from which they depend. Moreover, many of these claims are separately patentable. In particular, Claims 29, 30 and 31 are patentable for the same reasons that were described in connection with respective Claims 2, 3 and 4. This analysis will not be repeated for the sake of brevity.

Claims 33-40 Are Patentable

Independent Claim 33 is a method analog of Claim 26, and is patentable for the same reasons that were described above in connection with Claim 26. This analysis will not be repeated for the sake of brevity. Claims 34-40 are patentable at least per the patentability of Claim 33 from which they depend.

Moreover, many of these dependent claims are independently patentable. In particular, the Official Action has acknowledged that Claims 38 and 39 are independently patentable. Moreover, Claims 34, 35 and 36 are independently patentable for the same reasons that were described above in connection with Claims 2, 3 and 4. This analysis will not be repeated for the sake of brevity.

Finally, Claim 40 recites that prior to indexing, the FIFO memory is divided into up to the predetermined number of independent FIFO queues. Thus, Claim 40 is independently patentable for the same reasons that were described in connection with the recitations of a FIFO memory in Claim 1. This analysis will not be repeated for the sake of brevity.

Conclusion

Applicants again appreciate the thorough examination and the Examiner's indication that Claims 10-18, 20, 27, 30 and 39 are allowable. However, the analysis provided above has shown that Kumar does not describe or suggest many of the recitations of the independent and dependent claims. As was noted above, since Kumar includes an ATM switch with multiple memory modules, Kumar by definition includes memory modules, controllers, input networks, output networks and header processing circuits. However, these

elements of Kumar do not provide the same function or operational steps as the elements or steps of Claims 1-40, as was shown extensively by the above analysis. Accordingly, all of the pending claims are patentable over Kumar, and Applicants respectfully request allowance of the present application.

Respectfully submitted,

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